Comparator Design Strategy

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A comparator can have a single input terminal though most comparators have two input terminals. The input to comparators are analog signals and the output is a Boolean variable. For a single-input comparator, the output ideally goes high (low) if the input is above (below) a predetermined reference level and goes low (high) if the input is below a predetermined reference level. The symbols for a single-input and a two-input comparator are shown in Fig. 1. The corresponding ideal transfer characteristics for these comparators are shown in Fig. 2. Comparators can have either inverting or noninverting outputs. The transfer characteristics shown in Fig. 2 are those of noninverting comparators.

Fig. 1 Single-Input and Two-Input Comparators

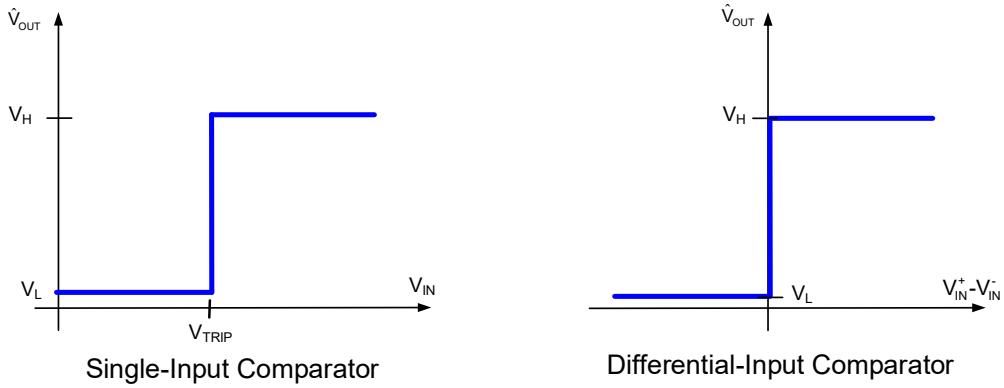

Fig. 2 Ideal Transfer Characteristics of Comparators

Circuit schematics of the most basic single-input noninverting and inverting comparators are shown in Fig. 3. It can be observed that these circuits are comprised of what is the most basic logical inverter. The trip point of the inverting comparator is equal to the trip-point voltage of the basic digital inverter and the trip point of the noniverting comparator is equal to the trip-point voltage of the first-stage digital inverter. Thus, in both cases, it is given by the expression

$$V_{TRIP} = \frac{\left(V_{THn}\right) + \left(V_{DD} + V_{THp}\right)\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

It can be observed that the trip point of these comparators is determined by the dimensions of the transistors and the device model parameters V_{THn}, V_{THp}, μ_n, and μ_p. Though the dependence on the device dimensions is attractive, the dependence on the model parameters is unattractive because they are highly process and temperature dependent. For these reasons, these single-ended comparators are useful only when the accuracy required for the trip-point voltage is low.

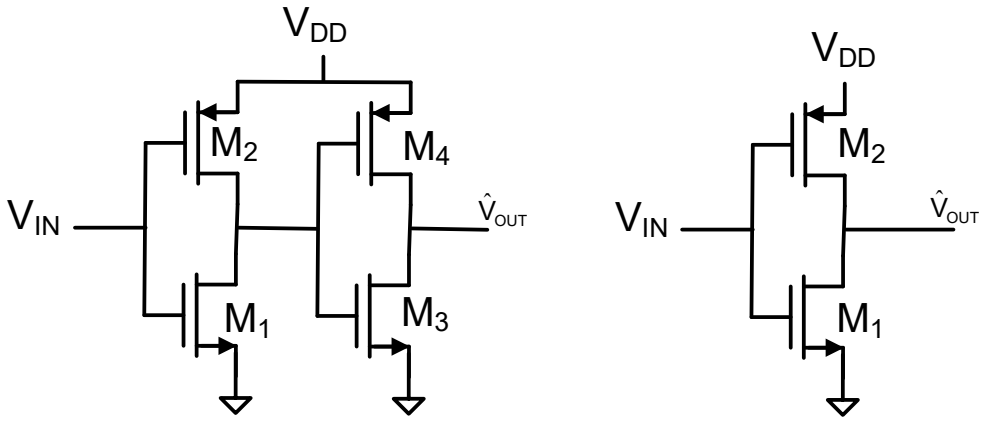

Fig. 3 Circuit Schematic of Basic Noninverting and Inverting Single-Input Comparator

Almost any differential-input operational amplifier can be used as a comparator. Since operational amplifiers are designed to operate in a feedback configuration, they require frequency compensation to provide stable operation when feedback is applied. This compensation limits the high frequency gain and the speed of the operational amplifier and may also increase power requirements. Since comparators are not intended to be used in a feedback configuration, they do not require compensation. So using operational amplifiers as comparators is often not a practical solution.

Some comparators operate asynchronously with the static transfer characteristics shown in Fig. 2 and others are clocked and provide an output only on either the rising edge or falling edge of a clock signal. Almost all operational amplifiers can be modified to serve as asynchronous comparators by simply removing all compensation capacitors. Removing the compensation capacitors will also improve the speed of the resulting comparator compared to what it would be if the compensation capacitors were left intact.

One of the most basic differential input asynchronous comparators is shown in Fig. 4. This is the noninverting configuration. An inverting configuration can be obtained by simply interchanging the labeling of the two input voltages. Transistors $M_1..M_7$ comprise what is often referred to as the static portion of the 7-T (seven-transistor) op amp. This is obtained by simply removing the compensation capacitor in the basic 7-T op amp architecture.

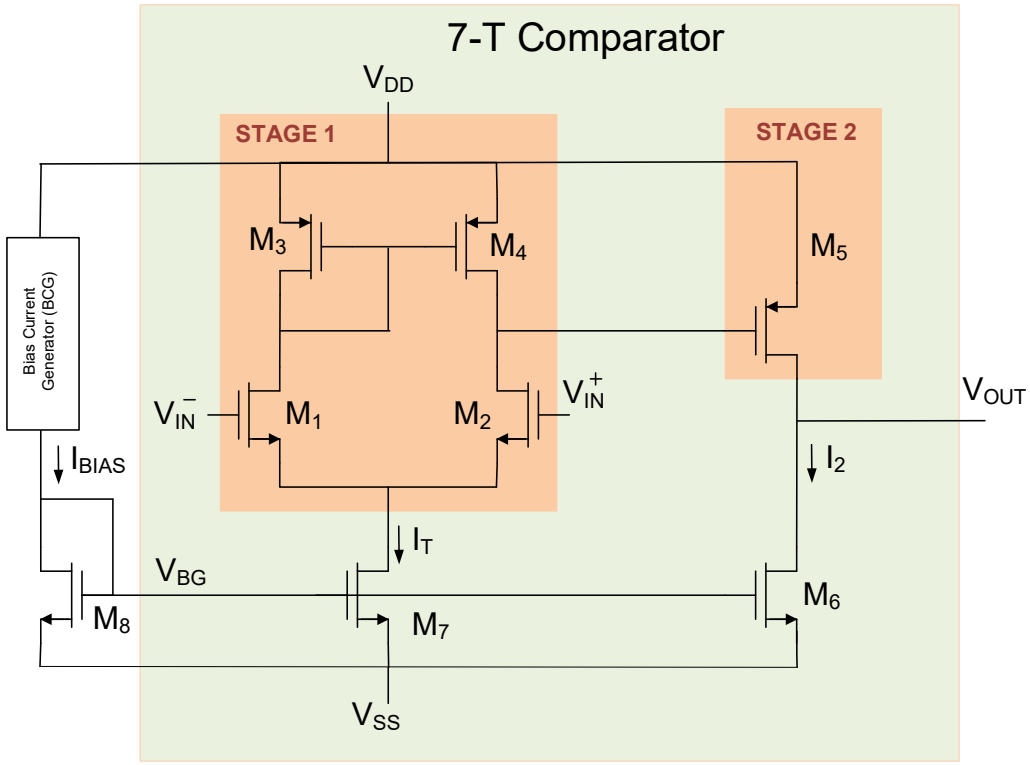

Fig. 4 Basic two-stage asynchronous comparator

The reader is referred to the companion op amp design document for a systematic procedure for designing this comparator. The only difference when designing the 7-T comparator and the 7-T op amp is that the compensation step is simply eliminated when using this structure as a comparator.

The slope in the output characteristics of the 7-T comparator can be increased by following the 7-T comparator with a digital inverter as shown in Fig. 5 . Neither the device sizing nor the trip point is very critical when adding the digital inverter.

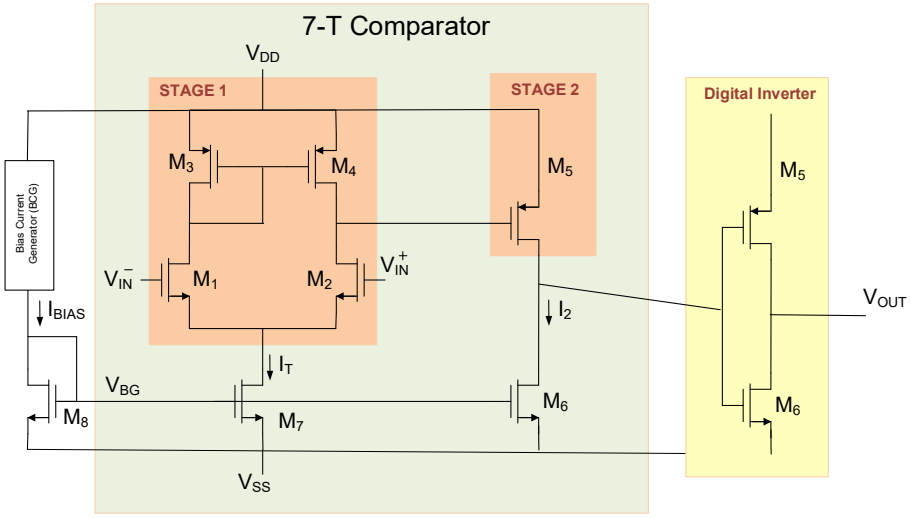

Fig. 5 9-T Comparator with Enhanced Gain

Much like the op amp, the offset voltage of a comparator is often critical and it is given by the same expression that were presented for the operational amplifier. The effects of offset voltage in a comparator are depicted in Fig. 6 for a positive offset. The offset voltage is a random variable and can be negative as well. The only way to reduce the offset voltage in this structure is to put a lot of area into the transistors M_1-M_4. There are other ways to reduce the offset voltage by modifying the comparator structure but those will not be addressed in this document.

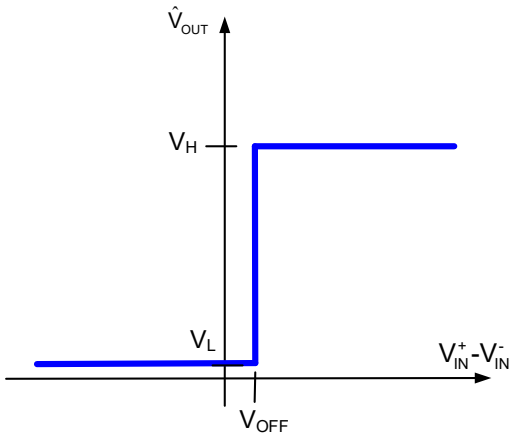

Fig. 6 Effects of Offset Voltage on 7-T Comparator

If an application requires a single-ended comparator, the differential input comparator with one of the inputs connected to a reference voltage source will provide the same basic functionality as the single-input comparators depicted in Fig. 3. The differential input comparator may be less sensitive to process and temperature variations than the single-input comparators shown in Fig. 3.

Clocked comparators are widely used as well, particularly when a comparator is required in a synchronous application. The asynchronous comparator discussed above consumes power continuously. Clocked comparators often only consume energy when they are doing a comparison. But offset voltages are often more challenging to address with clocked comparators. Some clocked comparators have inputs that go first through a continuous-time pre-amplifier before entering the clocked stage. This approach can reduce the offset voltage concerns and/or improve speed but at the expense of additional power dissipation. There are quite a few different clocked comparator architectures that have been proposed but a discussion of clocked comparators is beyond the scope of this document.

Layout of differential input comparators should follow the same guidelines that were presented in the companion operational amplifiers document and will not be repeated here.